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EXAMINER	
DU, THUAN N	
ART UNIT	PAPER NUMBER
2116	

DATE MAILED: 09/22/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	**Application No.** 10/022,208	**Applicant(s)** OH, JANG GEUN	
	Examiner Thuan N. Du	**Art Unit** 2116	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *28 June 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-21 and 23-25* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-8 and 10-21* is/are rejected.

7)☒ Claim(s) *9 and 23-25* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1)☐ Notice of References Cited (PTO-892)

2)☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)

3)☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.

4)☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .

5)☐ Notice of Informal Patent Application (PTO-152)

6)☐ Other: _____.

DETAILED ACTION

1. It is hereby acknowledged that the following papers have been received and placed of record in the file: Amendment (dated 6/28/05).

2. Claim 22 has been cancelled. Claims 1-21 and 23-25 are presented for examination.

3. The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

4. The rejections are respectfully maintained and reproduced infra for applicant's convenience.

Claim Rejections - 35 USC § 103

5. Claims 1-3 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yeh in view of Weidner.

6. Regarding claim 1, Yeh teaches a bus clock controlling method (Column 3, Lines 28-32) in a computer (Figure 1, Item 10; Column 2, Line 62), comprising:

setting a throttle rate of a clock to a predetermined initial value (Figure 2, Item 100; Column 4, Lines 49-53), the clock being used for a data bus (Figure 1, Item 32; Column 3, Lines 2-5) connected between a CPU (Figure 1, Item 20; Column 2, Lines 66-67) and a controlling device (Figure 1, Item 30., Column 2, Line 67);

detecting a user's pressing of a button (Figure 2, Item 102; Column 4, Lines 96-58) if a present power source is at least one battery column 1, Lines 16-18); and

adjusting the set throttle rate using the controlling device (Column 4, Lines 62-63; Column 5, Lines 2-3, 17-19) according to the user's button press (Figure 2; Item 104; Column 4, Lines 59-61).

Yeh teaches of adjusting the bus clock frequency based upon a user's button press instead of the remaining battery capacity.

Weidner teaches:

detecting a remaining battery capacity (Column 5, Lines 39-41);

adjusting the set throttle rate according to the detected remaining battery capacity (Column 5, Lines 42-45).

The motivation behind the device disclosed by Weidner is the understanding that when power resources are limited, there is an important goal of maximizing power usage. Weidner states that generating a clock of a lower frequency will conserve power (Column 5, Lines 35s39).

It would have been obvious to a person of ordinary skill in the art to modify Yeh's ability to set a bus clock rate based upon user interaction with the method of varying clock rates automatically based upon the remaining amount of power available to a system as taught by Weidner. This combination would have resulted in the mutual goal of maximizing the usage of a power supply by varying the bus clock rate.

7. Regarding claim 2, Weidner further teaches that the adjusting step increases the set throttle rate as the detected remaining battery capacity decreases (Column 5, Lines 42-45; a decrease in clock rate is equivalent to an increase in throttle rate).

8. Regarding claim 3, Yeh further teaches that the adjusting step selects one value appropriate to the detected remaining battery capacity among a plurality of throttle rates preset in

reverse proportion to different remaining battery capacities (Figure 2, Items 114l and 114h; the range of values detected can be one of only two values, low and high which are further tied to a corresponding and predefined frequency rate, wherein the clock rate is in reverse proportion to the throttle rate).

9. Claims 4 is rejected under 35 U.S.C. 103(a) as being unpatentable over Yeh in view of Weidner applied to claim 1 above and further in view of Young.

10. Regarding claim 4, Yeh and Weidner fail to teach of using a bridge controller as a controlling device.

Young teaches a controlling device is a bridge controller in a computer (Column 1, Lines 20-23).

Young is similarly motivated in providing a method for "dynamically controlling clock speed on a bus system that does not require human intervention"' (Column 2, Lines 41-42). His justification for this is that "supplying a full speed clock at all times is energy efficient"' (Column 1, Lines 50-5 1). PCI systems are widely used in computers and Young demonstrates a "typical PCI system"' (Column 1, Lines 17-18) incorporates a bridge circuit. Therefore, it would have been obvious to a person of ordinary skill in the art to use a bridge controller as a controlling device, so that the advantages of combining Yeh and Weidner can be used for a PCI system.

11. Claims 5-7 and 17-20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yeh in view of Atkinson.

12. Regarding claim 5, Yeh teaches a bus clock controlling method (Column 3, Lines 28-32) in a computer (Figure 1, Item 10; Column 2, Line 62), comprising:

setting a throttle rate of a clock to a predetermined initial value (Figure 2, Item 100; Column 4, Lines 49-53), the clock being used for a data bus (Figure 1, Item 32; Column 3, Lines 2-5) connected between a CPU (Figure 1, Item 20; Column 2, Lines 66-67) and a controlling device (Figure 1, Item 30; Column 2, Line 67);

detecting the pressing of a button by a user (Figure 2, Item 102; Column 4, Lines 56-58)

adjusting the set throttle rate using the controlling device (Column 4, Lines 62-63; Column 5, Lines 2-3, 17-19) according to the user's button press (Figure 2; Item 104; Column 4, Lines 59-61).

Yeh teaches of adjusting the bus clock frequency based upon the pressing of a button by a user rather than the load on the CPU and, though he notes the inverse relationship between bus clock frequency and power consumption performance, does not teach of adjusting the rate in reverse proportion to the load of the CPU.

Atkinson teaches:

detecting a present load of the CPU (Column 5, Lines 5-7);

adjusting the set throttle rate in reverse proportion to the present CPU load (Column 5, Lines 10-17).

The motivation for the device disclosed by Atkinson lies in the amount of power needed to supply a portable computer (Column 1, Lines 56-61). Atkinson attempts to extend the battery life in a portable computer by adjusting the clock frequency based upon the activity of the system.

Both Yeh and Atkinson offer ways of reducing power consumption based upon adjusting clock frequencies. Incorporation of Atkinson into Yeh would have created a system that accurately optimizes a bus clock according to system activity rather than user interaction. Therefore, it would have been obvious to a person of ordinary skill in the art to combine the bus clock varying system based upon user interactions described by Yeh with the clock adjusting system based upon system activity described by Atkinson to take advantage of its accurate clock optimization technique.

13. Regarding claim 6, Yeh further teaches that the adjusting step is conducted only when a present power source is at least one battery (Column 1, Lines 16-18).

14. Regarding claim 7, Yeh further teaches that the adjusting step includes selecting a new throttle rate appropriate to the detected CPU load from a plurality of throttle rates preset in reverse proportion to different CPU loads (Figure 2, Items 1 141 and 1 14h; the range of values detected can be one of only two values, low and high which are further tied to a corresponding and predefined frequency rate).

15. Regarding claim 17, Yeh teaches a bus clock controlling method (Column 3, Lines 28-32) in a portable computer (Figure 1, Item 10; Column 2, Line 64), comprising:

setting a throttle rate of a clock to a predetermined initial value (Figure 2, Item 100; Column 4, Lines 49-53), the clock being used for a data bus (Figure 1, Item 32; Column 3, Lines 2-5) connected between (Column 3, Lines 5-8) a controlling device (Figure 1, Item 30; Column 2, Line 67) and a selected one of a plurality of devices (Figure 1, Item 50; Column 3, Line 1) associated with the portable computer;

detecting (Figure 1, Item 78; Column 4, Lines 41-42) a condition of a prescribed criteria

(Figure 2, Item 1 12; Column 5, Lines 21-23) of the portable computer if a present power source is a battery (Column 1, Lines 16-18); and

adjusting the set throttle rate using the controlling device (Column 4, Lines 62-63; Column 5, Lines 2-3, 17-19) according to the detected condition (Figure 2, Item 118; Column 6, Lines 1-2), wherein the detected condition is within a range of values for the prescribed criteria (Figure 2, Items 1141 and 114h; Column 5, Lines 22-24; the range of values detected can be one of only two values, low and high).

Yeh does not disclose the prescribed criteria being either the condition of a remaining battery or a CPU load.

Atkinson teaches:

detecting a condition of CPU load (Column 5, Lines 5-7).

The motivation for combining Yeh with Atkinson can be seen above in the Claim 5 rejection.

16. Regarding claim 18, Yeh teaches that the selected device is a peripheral device (Figure 1, Item 60; Column 3, Line 1; the video card is peripheral by being attached yet not integral to the functioning of the CPU), and wherein the predetermined initial value is a smallest throttle rate (Figure 2, Item 100; Column 4, Lines 49-55).

17. Regarding claim 19, Yeh further discloses that the adjusting step selects a rate corresponding to the detected condition among a plurality of prescribed throttle rates that each correspond to mutually exclusive sets of values of the detected condition within the range of values for the prescribed criteria (Figure 2, Items 1141 and 114h; Column 5, Lines 22-24; the range of values detected can be one of only two values, low and high).

18. Regarding claim 20, Atkinson further teaches that each of the plurality of prescribed throttle rates increases as the detected condition decreases within the range (Figure 4, Items 206 and 212; column 7, Lines 34-38 and 45-50).

19. Claims 8, 11, 16 and 21 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yeh in view of Weidner, and further in view of Atkinson.

20. Regarding Claim 8, Yeh teaches a computer (Figure 1, Item 10; Column 2, Line 62), comprising:

a CPU that processes (Figure 1, Item 20; Column 2, Line 66-67);

a first controller (Figure 1, Item 30; Column 2, Line 67) coupled to the CPU via a data bus (Figure 1, Item 32; Column 3, Lines 3-4), and configured to provide a throttled clock (Column 3; Lines 30-32) to the data bus (Column 6, Lines 15-19) according to a throttle rate;

a clock generator (Figure 1, Item 40; Column 3, Line 11) coupled to the CPU (Figure 1, Item 34; Column 3, Line 13) and the first controller (Figure 1, Item 34; Column 3, Line 14), and configured to generate a clock for the CPU and the first controller (Column 3, Lines 11-14);

a detector (Figure 1, Item 78; Column 4, Lines 41-42) detecting a variable (Figure 1, Item 75a; Column 4, Lines 25-27), wherein the variable is whether or not a user has pressed a button.

a second controller (Figure 1, Item 70; Column 3, Lines 1-2) coupled to receive the detected variable (Figure 1, Item 75; Column 4, Lines 23-27), configured to determine the throttle rate according to the detected variable (Figure 2, Item 1 12; Column 5, Lines 22-24), and

further configured to output the throttle rate to the first controller, wherein the throttled clock is configured to have a different value than the clock (obviously the adjusted clock has a different value than the original clock).

Yeh teaches a variable that is the user's button press rather than the CPU load or remaining battery capacity. Additionally,

Weidner teaches:

a detector detecting a variable, wherein the variable is a remaining battery capacity (Weidner, Column 5, Lines 39-41).

a second controller coupled to receive the detected variable, configured to determine the throttle rate according to the detected variable and further configured to output the throttle rate to the first controller (Column 5, Lines 39-45).

The motivation for combining Yeh with Weidner can be seen above in the Claim 1 rejection.

Atkinson teaches:

a detector detecting a variable, wherein the variable is a load of the CPU (Column 5, Lines 5-7).

The motivation for combining Yeh with Atkinson can be seen above in the Claim 5 rejection.

Atkinson and Weidner do not teach of considering the valuable being a remaining battery capacity or a load of the CPU. However, it would have been obvious to a person of ordinary skill in the art, recognizing that both the remaining battery capacity and the CPU load are factors which may be considered as a reason for altering a bus clock frequency to save power, to create a

system that can vary the bus clock frequency based upon the CPU load or the remaining battery capacity.

21. Regarding claim 11, Weidner further teaches that the throttle rate increases as a value of the detected variable decreases (Column 5, Lines 42-45; a decrease in clock rate is equivalent to an increase in throttle rate).

22. Regarding claim 16, Yeh teaches a bus clock controlling method (Column 3, Lines 28-32) in a computer (Figure 1, Item 10; Column 2, Line 62), comprising:

setting a throttle rate of a clock to a predetermined initial value (Figure 2, Item 100; Column 4, Lines 49-53), the clock being used for a data bus (Figure 1, Item 32; Column 3, Lines 2-5) to which both a CPU (Figure 1, Item 20; Column 2, Lines 66-67) and a controlling device (Figure 1, Item 30; Column 2, Line 67) are connected;

detecting the pressing of a button by a user (Figure 1, Item 78; Column 4, Lines 41-42) if a present power source is a battery (Column 1, Lines 16-18); and

adjusting the set throttle rate according to the detected user's button pressed (Figure 2; Item 104; Column 4, Lines 59-61), wherein the clock is provided to the controlling device (Figure 1; Item 34), and wherein the throttle rate is set independently of the clock (Column 5, Lines 40-41).

Yeh does not teach the detection of remaining battery capacity or the CPU load or the adjustment to the throttle rate based upon the remaining battery capacity and the CPU load

Weidner teaches:

detecting a remaining battery capacity (Column 5, Lines 39-41); and

adjusting the set throttle rate according to the detected remaining battery capacity (Column 5, Lines 42-45).

The motivation for combining Weidner and Yeh can be seen in the above claim 1 rejection.

Atkinson teaches:

detecting a load of the CPU (Column 5, Lines 5-7).

adjusting the set throttle rate according to the detected CPU load (Column 5, Lines 10-17).

The motivation for combining Yeh with Atkinson can be seen above in the Claim 5 rejection.

Atkinson and Weidner do not teach of considering the variable being a remaining battery capacity and a load of the CPU. However, it would have been obvious to a person of ordinary skill in the art, recognizing that both the remaining battery capacity and the CPU load are factors which may be considered as a reason for altering a bus clock frequency to save power, to create a system that can vary the bus clock frequency based upon the CPU load and the remaining battery capacity.

23. Regarding claim 21, Yeh teaches a bus clock controlling method (Column 3, Lines 28-32) in a computer (Figure 1, Item 10; Column 2, Line 62), comprising:

setting a throttle rate of a clock to a predetermined initial value (Figure 2, Item 100; Column 4, Lines 49-53), the clock being used for a data bus (Figure 1, Item 32; Column 3, Lines 2-5) to which both a controlling device (Figure 1, Item 30; Column 2, Line 67) and a peripheral device are connected;

detecting the pressing of a button by a user (Figure 1, Item 78; Column 4, Lines 41-42).

adjusting the set throttle rate using the controlling device (Column 4, Lines 62-63; Column 5, Lines 2-3, 17-19) according to the user's button press (Figure 2; Item 104; Column 4, Lines 59-61).

Yeh teaches detecting a button press by a user and determination therefrom of a throttle rate instead of by a load on the CPU or a remaining battery capacity.

Weidner teaches:

detecting a remaining battery capacity (Weidner, Column 5, Lines 39-41).

adjusting the set throttle rate in reverse proportion to the detected remaining battery capacity (Column 5, Lines 42-45; a decrease in clock rate is equivalent to an increase in throttle rate).

The motivation for combining Yeh with Weidner can be seen above in the Claim 1 rejection.

Atkinson teaches:

detecting a present load of the CPU (Column 5, Lines 5-7).

adjusting the set throttle rate in reverse proportion to the detected present CPU load (Column 5, Lines 10-17).

The motivation for combining Yeh with Atkinson can be seen above in the Claim 5 rejection.

Atkinson and Weidner do not teach of varying a bus clock frequency based upon at least one member chosen from the remaining battery capacity or load of the CPU. However, it would have been obvious to a person of ordinary skill in the art, recognizing that both the remaining

battery capacity and the CPU load are factors which may be considered as a reason for altering a bus clock frequency to save power, to create a system that can vary the bus clock frequency based upon the CPU load or the remaining battery capacity.

24. Claim 10 is rejected under 35 U.S.C. 103(a) as being unpatentable over Yeh, Weidner and Atkinson and further in view of Young.

25. Regarding claim 10, Weidner further teaches that the second controller determines the throttle rate in reverse proportion to the detected variable (Figure 2, Items 114l and 114h; Column 5, Lines 22-24; the range of values detected can be one of only two values, low and high).

Weidner and Yeh do not teach of using a bridge controller as the first controller.

Young teaches that the controller is a bridge controller (Column 1, Lines 20-23).

26. Claims 12-15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yeh, Weidner and Atkinson and further in view of Parrish.

27. Regarding claim 12, Atkinson further teaches:

the second controller comprises:

at least one comparator coupled to receive the detected variable from the detector (the variable is used in a comparison, therefore there must be a comparator that receives the detected variable so that the comparison may be performed), configured to compare the detected variable to a plurality of predetermined values, and further configured to output a result of the

corresponding plurality pf comparisons (Figure 4, Items 206 and 212; Column 7, Lines 34-38 and 45-50).

Weidner teaches:

a host clock throttle configured to output the throttle rate to the first controller (Column 5, Lines 39-45).

Weidner and Atkinson do not teach a host clock throttle that receives the plurality of compassions and a power mode signal.

Panish teaches:

a host clock throttle coupled to receive the plurality of comparisons and a power mode signal (Columns 1 and 2, Lines 64-67 and 1, respectively).

Parrish states that "Controller chips that operate at high clock speeds typically consume more power than controller chips running at lower clock speeds" which "may deplete power sources used to power portable computers'" (Column 1, Lines 25-31). He states that while power conservation is important, "when power is supplied by an AC source such as the electrical outlet 130, power conservation may not be an important issue, and it may be desirable to operate the graphics adapter 110 at a higher frequency to provide better graphics performance" (Column 2, Lines 38-42).

It would have been obvious to a person of ordinary skill in the art to further include a power mode signal that identifies the power source used in a system as described by Parrish with the combination of Yeh, Weidner and Atkinson because it would have afforded it the additional advantage of deciding whether or not power conservation is really necessary before altering the speed of the bus.

28. Regarding Claim 13, Weidner further teaches that the at least one comparator comprises a remaining battery capacity comparator, and wherein the detected variable is the remaining battery capacity (Column 5, Lines 42-45; the comparison occurs as the controller selects an output frequency based upon power remaining).

29. Regarding claim 14, Atkinson further teaches that the at least one comparator comprises a CPU load comparator (Column 7, Lines 19-22), and wherein the detected variable is the load of the CPU (Column 7, Line 8).

30. Regarding claim 15, Atkinson teaches that the at least one comparator comprises a CPU load comparator (Column 7, Lines 19-22).

Weidner teaches the at least one comparator comprises a remaining battery capacity comparator (Column 5, Lines 42-45).

Atkinson and Weidner do not teach of the at least one comparator comprising a CPU load comparator and a remaining battery capacity comparator. However, it would have been obvious to a person of ordinary skill in the art, recognizing that both the remaining battery capacity and the CPU load are factors which may be considered as a reason for altering a bus clock frequency to save power, to use the at least one comparator to consider both the CPU load and the remaining battery capacity when deciding how to adjust the clock speed of the bus.

Allowable Subject Matter

31. Claims 9 and 23-25 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Response to Arguments

32. Applicant's arguments filed June 28, 2005 have been fully considered but they are not persuasive.

In response to applicant's argument that Yeh does not teach or suggest adjusting the set throttle using the controlling device, examiner respectfully disagrees. Yeh teaches that the event controller 70 sends an interrupt signal to the controlling device 30 (Column 4, Lines 62-63) then wait for suspend signal from the controlling device 30 (Column 5, Lines 2-3). After receiving the suspend signal and determined that the suspend signal is TRUE (Column 5, Lines 17-19), the event controller adjusts the set throttle (Column 5, Lines 25-27). Therefore, the controlling device 30, indirectly, adjusts the set throttle as claimed.

In response to applicant's argument that Weidner does not teach or suggest a throttle rate of a clock for a bus, examiner respectfully submits that Yeh was relied upon to teach the limitation (Yeh, Column 3, Lines 2-5, 29-33).

In response to applicant's argument that Atkinson does not teach or suggest the features of detecting a present load of the CPU and adjusting the set throttle rate in reverse proportion to the present CPU load, examiner respectfully disagrees. Atkinson teaches that the CPU load is monitored and detected (Column 5, Lines 12-13), and the throttle rate is adjusted in reverse proportion to the present CPU load (Column 5, Lines 10-12).

Conclusion

33. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

34. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Thuan N. Du whose telephone number is (571) 272-3673. The examiner can normally be reached on Monday-Friday: 9:30 AM - 6:00 PM, EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Lynne H. Browne can be reached on (571) 272-3670.

Central TC telephone number is (571) 272-2100.

The fax number for the organization is (571) 273-8300.

35. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished

applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll free).

Thuan N. Du
September 17, 2005